LP5952 Evaluation Board

National Semiconductor
Application Note 1531
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April 3, 2008

Introduction

This evaluation board is designed to enable independent evaluation of the LP5952 electrical performance. Each board is pre-assembled and tested in the factory.

The evaluation kits are available in four output voltage options for the micro SMD package: LP5952TL-1.2EV, LP5952TL-1.3EV, LP5952TL-1.5EV and LP5952TL-1.8EV and one output voltage option for the COL LLP package: LP5952LC-1.5EV. For other voltage options, the device can be ordered from LP5952 product folder on National's website.

The board contains the LP5952 and input and output capacitors connected to GND.

General Description

The LP5952 converts higher input voltages connected to the power input voltage pin V_{IN} to lower output voltages while consuming low quiescent current. The bias input voltage V_{BATT} supplies internal circuitry.

The LP5952 is capable of operating with input voltage ranges from $0.7V \leq V_{IN} \leq 4.5V$ and $2.5V \leq V_{BATT} \leq 5.5V$ for fixed output voltage options from 0.5V to 2.0V. The LP5952 can supply a maximum output current of 350mA and is particularly suitable for portable, battery-powered systems. It also features internal protection against short-circuit and over-temperature conditions.

The power input voltage applied between V_{IN} and GND should be at least 0.2V above the output voltage and the bias input voltage applied between V_{BATT} and GND should be at least 1.5V above the output voltage (with a minimum of 2.5V) to operate the device within operating conditions. Input connections should be kept reasonably short (<20cm) to minimise input inductance and ensure optimum transient performance.

ON/OFF control of the LP5952 is realized by a logic signal applied to the EN pin. To simplify the enabling of the device, a three pin jumper is provided on the evaluation board. The middle pin is directly connected to the EN pin of the device. A logic signal with a minimum of 1.0V to enable the device or with a maximum of 0.4V to disable the device can be directly connected to this jumper pin in the middle. Alternatively the middle pin can be shorted to the pin next to it to the left or to the right marked ON or OFF.

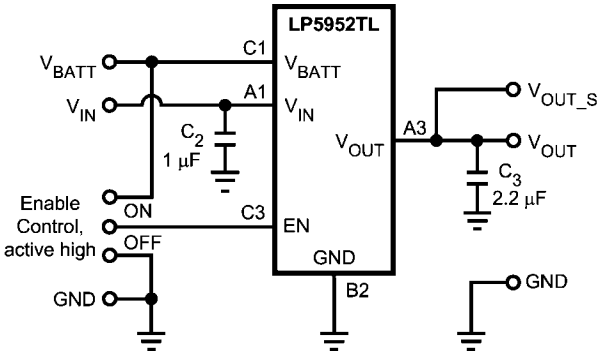
A load of up to 350mA maximum may be connected from the V_{OUT} pin to GND.

At the bottom of the board the output voltage option (1.2V, 1.3V, 1.5V, or 1.8V) is printed.

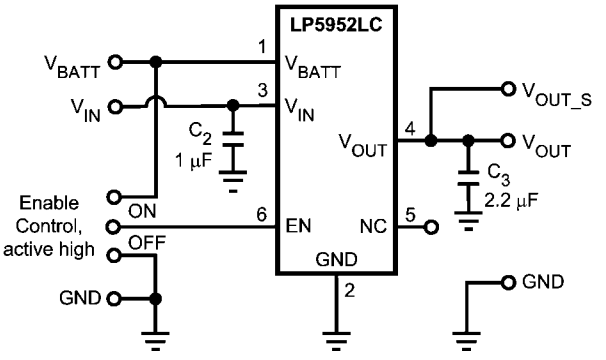
The V_{OUT_S} pin represents a sense path to the output voltage pin and can be used for more precise voltage measurements.

The schematic and board layout for both packages are shown below:

Schematic Diagram

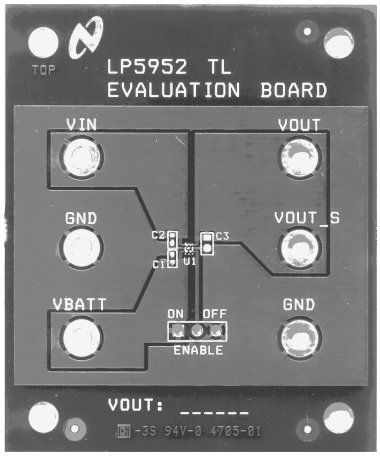


Evaluation Board Schematic (TL Package)



Evaluation Board Schematic (LC Package)

Evaluation Board Component and Pin Layout



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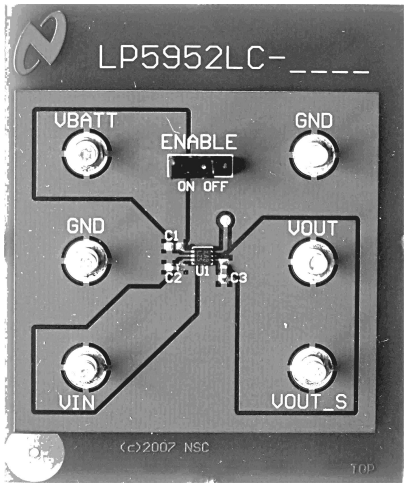
LP5952TL: TOP Side
Board Size: 50mm x 60mm



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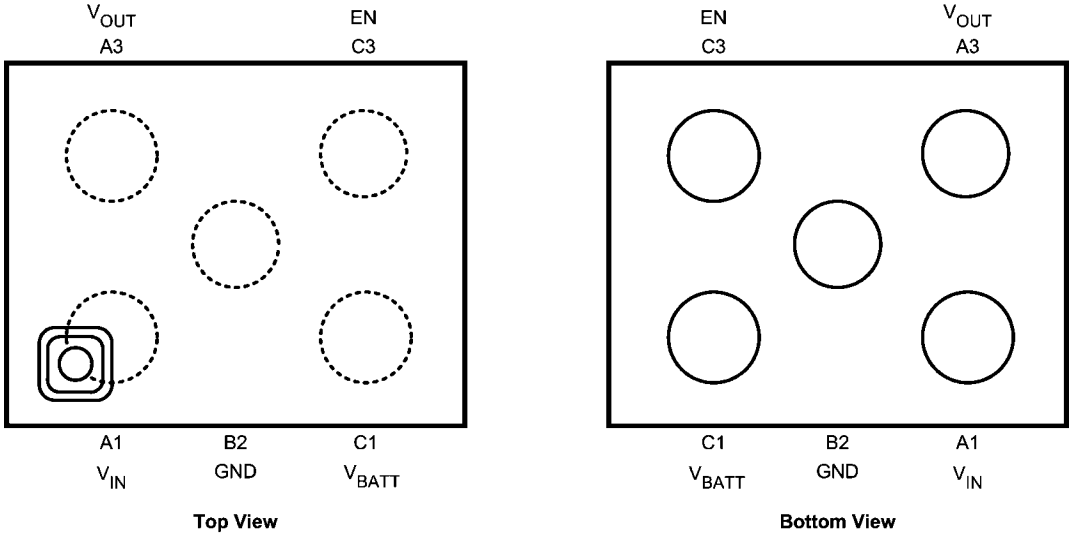
LP5952LC: TOP Side
Board Size: 50mm x 60mm

Connection Diagrams



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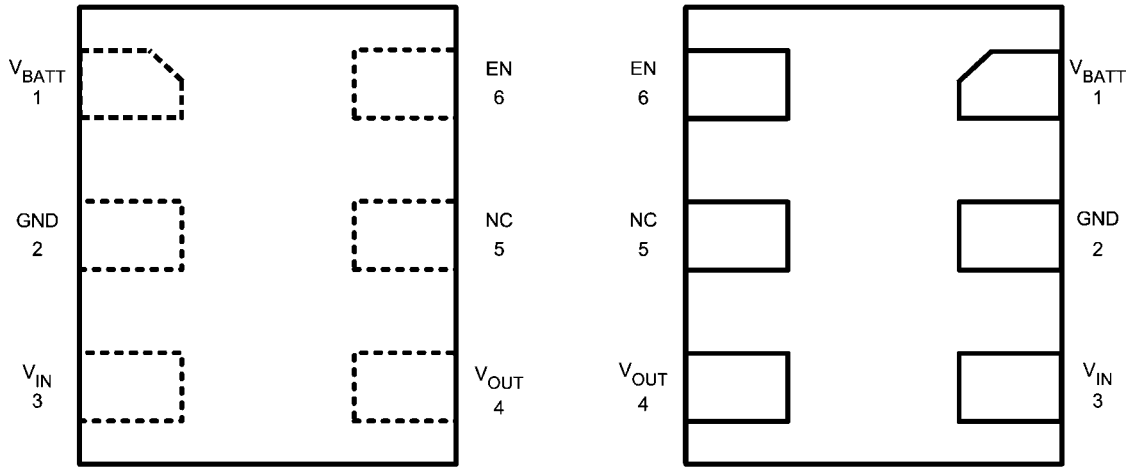
Connection Diagram 5-Bump Thin Micro SMD Package, Large Bump, 0.5mm Pitch



Connection Diagram 6-Pin Chip On Lead LLP Package, 0.5mm Pitch

Table 1: Pin Descriptions

Pin Number Micro SMD	Pin Number LLP	Name	Description
A1	3	V_{IN}	Power input voltage; input range: 0.7V to 4.5V, $V_{IN} \leq V_{BATT}$
A3	4	V_{OUT}	Regulated output voltage
B2	2	GND	Ground
C1	1	V_{BATT}	Bias input voltage; input range: 2.5V to 5.5V
C3	6	EN	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Short to V_{BATT} using attached jumper for normal operation.
	5	NC	No internal connection

Table 2: Bill of Materials

Item	Description	Amount	Footprint	Mfg., Part Number
C1	C_{BATT}, optional, not needed, capacitor at V_{BATT}	0	0402 / 0201	
C2	C_{IN}, ceramic capacitor, 1µF, X5R at V_{IN}	1	0402 / 0201	TDK, C1005X5R1A105K or Taiyo Yuden, LMK105BJ105KV-F
C3	C_{OUT}, ceramic capacitor, 2.2µF, X5R at V_{OUT}	1	0603 / 0402	TDK, C1608X5R0J225K or Taiyo Yuden, JMK105BJ225MV-F
U1	Linear Regulator LP5952TL or LP5952LC	1	5-bump micro SMD: TLA05Z1A or 6-pin COL LLP: LCA06B	National Semiconductor, LP5952TL-x.x or LP5952LC-1.5
V_{IN}, V_{BATT}, V_{OUT_S}, V_{OUT}, GND	Test pins	6		Cambion, 160-1026-02-05
ENABLE	3 pin jumper for enable function	1		

Application Hints

DUAL RAIL SUPPLY

The LP5952 requires two different supply voltages:

•V_{IN}, the power input voltage, is regulated to the fixed output voltage

•V_{BATT}, the bias input voltage, supplies internal circuitry.

It's important that V_{IN} does not exceed V_{BATT} at any time. If the device on the evaluation board is used in the typical post regulation application as shown in FIGURE 1 of the datasheet using a DC-DC converter to generate V_{IN} out of V_{BATT}, the sequencing of the two power supplies is not an issue as V_{BATT} supplies both, the DC-DC regulator and the LP5952. The output voltage of the DC-DC regulator will take some time to rise up and supply V_{IN} of LP5952. In this application V_{IN} will always ramp up more slowly than V_{BATT}.

In case V_{IN} is shorted to V_{BATT}, the voltages at the two supply pins will ramp up simultaneously causing no problem.

If the LP5952 evaluation board is used stand alone, two independent supplies are connected to the LP5952. Therefore special care must be taken to guarantee that **V_{IN} is always ≤ V_{BATT}**.

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

The allowable power dissipation for the device in a given package can be calculated using the following equation:

$P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$

With a θ_{JA} = 95°C/W, the device in the 5 bump micro SMD package returns a value of 1053mW with a maximum junction temperature of 125°C at T_A of 25°C or 421mW at T_A of 85°C.

With a θ_{JA} = 150°C/W, the device in the 6-pin COL LLP package returns a value of 667mW with a maximum junction temperature of 125°C at T_A of 25°C or 267mW at T_A of 85°C.

The actual power dissipation across the device can be estimated by the following equation:

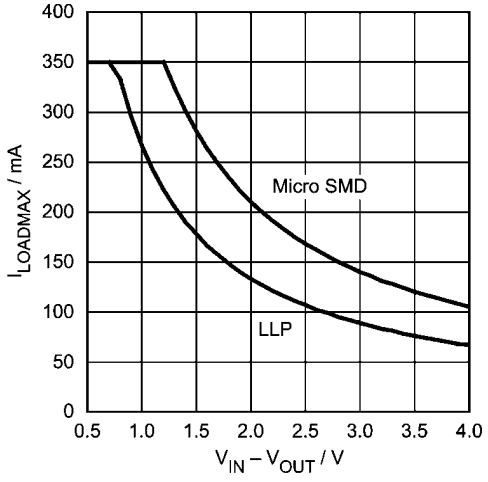
$P_D \approx (V_{IN} - V_{OUT}) * I_{OUT}$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application. As an example for the micro SMD package, to keep full load current capability of 350mA for a 1.5V output voltage option at a high ambient temperature of 85°C, V_{IN} has to be kept ≤ 2.7V:

$V_{IN} \leq P_D / I_{OUT} + V_{OUT}$ = 421mW / 350mA + 1.5V = 2.7V.

The figure below shows the output current derating due to these considerations:

Output Current Derating



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Maximum Load Current vs V_{IN} - V_{OUT},
T_A = 85°C, $\theta_{JA(MICROSMD)}$ = 95°C/W, $\theta_{JA(LLP)}$ = 150°C

The typical contribution of the bias input voltage supply V_{BATT} to the power dissipation can be neglected: $P_{D\_VBATT} = V_{BATT} * I_{Q\_VBATT}$ = 5.5V * 50µA = 0.275mW typical.

EXTERNAL CAPACITORS

If the LP5952 evaluation board is used stand alone (V_{IN} and V_{BATT} directly connected to a dual power supply), an input capacitor at V_{IN} (C2) is required for stability. A ceramic capacitor of 1.0µF is recommended and assembled at the power input pin V_{IN}.

A capacitor at V_{BATT} (C1) is not required if the distance to the supply does not exceed 5cm. Therefore no capacitor is assembled by default, but a footprint is provided on the evaluation board.

At the output (C3) a 2.2µF ceramic capacitor is recommended and assembled.

For further details on recommended capacitors and capacitor characteristics please see bill of materials above and the datasheet.

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
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